REMARKS

Claims 4-12 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The examiner appears to have misunderstood claim 4 and the accompanying specification. Figure 1(c) shows two side wall structures 110 and 120. In claim 4, the first sidewall structure refers to 120 and the second sidewall structure refers to 110. As clearly shown in Figure 1(C) the second width 102 of the second sidewall structure 110 is less than the first width 101 of the first sidewall structure 120. This is exactly what is described in claims 4-12.

Claims 1-6, 8-10 and 12 were rejected under 35 U.S.C. 102(b) as being anticipated by Ogoh; and Claims 7 and 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ogoh in view of Wang.

Claims 1-6 and claim 8 were amended to include the limitation of a single sidewall layer sidewall structure. For a 102(b) rejection to be valid each and every limitation of the instant invention must be found in the referenced art. The Ogoh patent (US 5,254,866) patent describes sidewall structures with different widths and multiple layers. The amended claims 1-8 all describe a method for forming single layer sidewall structures with varying widths. Since this limitation is not found in the Ogoh patent then claims 1-8 are allowable over all the cited art. Claims 9 –12 includes the limitation of using the source drain masking layer to mask one of the transistor structures while the other sidewall structure is etched. This limitation is not found in either the Ogoh patent not the Wang et al patent and claims 9-12 are allowable over all the cited art.

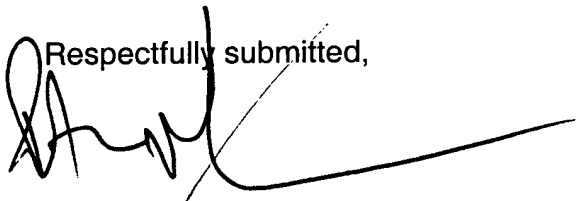
In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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Version with Markings to Show Changes Made

1(Amended). A method of forming a CMOS sidewall spacer, comprising the steps of:

forming a PMOS transistor gate structure on a n-type region of a semiconductor substrate;

forming a NMOS transistor gate structure on a p-type region of said semiconductor substrate;

forming single layer sidewall structures adjacent to said NMOS transistor gate structure and said PMOS transistor gate structure; and

etching said single layer sidewall structure adjacent to said NMOS transistor gate structure such that the width of the single layer sidewall structure adjacent to said NMOS transistor gate structure is less than the width of the single layer sidewall structure adjacent to said PMOS transistor gate structure.

2(Amended). The method of claim 1 wherein said etching of said single layer sidewall structure is an anisotropic etch.

3(Amended). The method of claim 1 wherein said single layer sidewall structure is a material selected from the group consisting of silicon nitride, silicon oxide, and silicon oxynitride.

4(Amended). A method for forming CMOS sidewall spacers, comprising the steps of:

providing a semiconductor substrate of a first conductivity type with a region of a second conductivity type;

forming a gate dielectric on said semiconductor substrate;

forming a conductive layer on said gate dielectric;

etching said conductive layer and said gate dielectric to form a first transistor gate stack with an upper surface on said semiconductor substrate of a first conductivity and a second transistor gate stack with an upper surface on said region of said semiconductor substrate of a second conductivity type;

forming at least one first single layer sidewall structure of a first width adjacent to said second transistor gate stack; and

forming at least one second single layer sidewall structure of a second width adjacent to said first transistor gate stack wherein said second width is less than said first width.

5(Amended). The method of claim 4 where said forming at least one first single layer sidewall structure of a first width comprises:

forming a single layer sidewall film over said semiconductor substrate; and

etching said single layer sidewall film using an anisoptropic etch such that all of said single layer sidewall film is removed from said upper surface of said first transistor gate stack and a portion of said single layer sidewall film is left adjacent to said second transistor gate stack.

6(Amended). The method of claim 5 where the single layer sidewall film is silicon nitride, silicon oxide, or silicon oxynitride.

8(Amended). The method of claim 4 where said forming at least one second single layer sidewall structure of a second width comprises:

providing a first transistor gate stack with at least one adjacent single layer sidewall film of a first width;

masking said second transistor gate stack using a source drain implant mask; and

etching said single layer sidewall film of a first width adjacent to said first transistor gate stack.